REMARKS/ARGUMENTS

Claims 1 and 4 are pending in this Application.

Claims 1 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Miyauchi (U.S. Patent No. 5,717,886). Applicant respectfully traverses the rejection of claims 1 and 4.

Claim 1 recites:

> "A data processing device comprising:
> a read-only memory;
> a flash memory capable of modifying information stored therein and adding information thereto;
> a central processing unit performing data processing using information stored in said read-only memory and said flash memory;
> an information storage area provided in said flash memory for storing predetermined modifiable information among the information used by said central processing unit for data processing;
> an address storage area provided in said flash memory for storing at least the address of the information stored in said information storage area; and
> an address-modification control unit for, after at least one of modification of modifiable information stored in said information storage area and addition of modifiable information to said information storage area, and in accordance with said one of the modification of the information and addition of the information, performing one of modification of the address of the information stored in said address storage area and addition of the address of the information to said address storage area; wherein
> the information used by said central processing unit for data processing can be freely modified or added; and
> **the address-modification control unit controls a function address table area and a variable address table area.**" (emphasis added)

Claim 4 recites:

> "A method in a data processing device comprising:
> a read-only memory;
> a flash memory capable of modifying information stored therein and adding information thereto;
> a central processing unit performing data processing using

information stored in said read-only memory and said flash memory;

an information storage area in said flash memory; and

an address storage area in said flash memory;

said method comprising the steps of:

storing in said information storage area predetermined modifiable information among the information used by said central processing unit for data processing;

storing in said address storage area at least the address of the information stored in said information storage area;

performing at least one of modification of modifiable information stored in said information storage area and addition of modifiable information to said information storage area; and

then, in accordance with said one of modification of the information and addition of the information, performing one of modification of the address of the information, stored in said address storage area and addition of the address of the information to said address storage area; wherein

whereby the information used by said central processing unit for data processing can be freely modified or added; and

the address storage area includes a function address table area and a variable address table area." (emphasis added)

Applicant's claim 1 recites the feature of "the address-modification control unit controls a function address table area and a variable address table area." Applicant's claim 4 recites the feature of "the address storage area includes a function address table area and a variable address table area." With the improved features of claims 1 and 4, Applicant has been able to provide a data processing device in which the main program and information regarding functions can be freely modified (see, for example, the fourth full paragraph on page 2 of the originally filed Specification).

The Examiner alleged in paragraph no. 7 on pages 6 and 7 of the outstanding Office Action that "the features upon which applicant relies (i.e., differentiate the information to be stored in the flash memory 104 into functions and variables) are not recited in the rejected claims." Applicant respectfully disagrees.

As noted by the Examiner, Applicant's claim 1 recites the feature of "the address-modification control unit controls a **function** address table area and a **variable** address

table area" (emphasis added) and Applicant's claim 4 recites the feature of "the address storage area includes a **function** address table area and a **variable** address table area" (emphasis added). That is, Applicant's claimed invention clearly stores the addresses of functions and the addresses variables differently, addresses of functions are stored in the function address table area and addresses of variables are stored in the variable address table. It cannot be more clear that Applicant's claimed invention differentiates the information in the flash memory into functions and variables.

The prior are clearly fails to teach or suggest (1) a function address table are; (2) a variable table address area; and (3) an address-modification control unit controlling the function address table area and the variable table address area.

The Examiner has alleged in paragraph no. 6 on pages 5 and 6 of the outstanding Office Action that Miyauchi teaches the function address table area and the variable address table area of the claimed invention. Applicant respectfully disagrees.

First, the Examiner alleged that **Figs. 20** and **21** of Miyauchi teach the function address table area and the variable address table area of the claimed invention. This is not correct.

As argued in the previous Amendment, filed February 4, 2004, Miyauchi is directed to determining a conversion table between **Logic Sector** Addresses (LSA) and **Physical Sector** Address (PSA) for any information that is stored in the flash memory **104**. The last paragraph of column 1 of Miyahichi states that "[c]onversion table **103** relates the logical sector address (LSA) sent from host unit **110** to the physical sector address (PSA) used inside semiconductor disk device **100**." That is, all of the information inside the semiconductor disk device **100** of Miyauchi has two addresses associated with it, an LSA and an PSA.

However, Miyauchi makes absolutely no indication that any of information stored inside the semiconductor disk device **100** shown in **Figs. 20** and **21** is differentiated into functions and variables and, certainly, fails to teach or suggest that the address of any of the information the inside the semiconductor disk device **100** is included in a function

address table area or a variable address table area.

In fact, nothing in Miyauchi can be construed to be a function address table area or a variable address table area. The LSA and PSA of Miyauchi clearly do not constitute a function address table area or a variable address table area.

Second, the Examiner alleged that **Figs. 6** and **7** of Miyauchi teach the function address table area and the variable address table area of the claimed invention. As argued above with respect to **Figs. 20** and **21** of Miyauchi, Miyauchi makes absolutely no indication that any of information stored inside the semiconductor disk device **100a** or flash memory **104a** shown in **Figs. 6** and **7** is differentiated into functions and variables and, certainly, fails to teach or suggest that the address of any of the information inside the semiconductor disk device **100a** or flash memory **104a** is included in a function address table area or a variable address table area.

Thus, Miyauchi clearly fails to teach or suggest the feature of "the address-modification control unit controls a function address table area and a variable address table area" as recited in Applicant's claim 1 or the feature of "the address storage area includes a function address table area and a variable address table area" as recited in Applicant's claim **4**.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 and 4 under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Miyauchi.

Accordingly, Applicant respectfully submits that AAPA and Miyauchi, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements and method steps recited in claims 1 and 4 of the present application.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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